AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

What is claimed is:

1. (Currently amended) An interface for receiving data from an image sensor having an imaging array and a clock generator for transfer to a processor system comprising:
   - a memory ~~means~~ for storing imaging array data and clocking signals at a rate determined by the clocking signals;
   - a signal generator ~~means~~ for generating a signal for transmission to the processor system in response to the quantity of data in the memory ~~means~~; and
   - a circuit ~~means~~ for controlling the transfer of the data from the memory ~~means~~ at a rate determined by the processor system.

2. (Currently amended) An interface as claimed in claim 1 wherein the memory ~~means~~ is a first-in first-out (FIFO) buffer.

3. (Currently amended) An interface as claimed in claim 2 wherein the signal generator ~~means~~ generates an interrupt signal for transmission to the processor system.

4. (Currently amended) An interface as claimed in claim 3 wherein the circuit ~~means~~ for controlling the transfer of the data includes:
   - a command decoder ~~means~~ for receiving address and command signals from the processor system;

- a configuration register ~~means~~ for storing configuration data for the FIFO buffer; and
- a read control ~~means~~ for controlling the read-out of the FIFO buffer.

5. (Currently amended) An interface as claimed in claim 4 wherein the interface further includes an array register ~~means~~ for determining the dimension of the imaging array data.

6. (Currently amended) An interface as claimed in claim 2 wherein the signal generator ~~means~~ generates a bus request signal for transmission to a bus arbitration unit for the processor system.

7. (Currently amended) An interface as claimed in claim 6 wherein the circuit ~~means~~ for controlling the transfer of the data further includes:
- a command decoder ~~means~~ for receiving address and command signals from the processor system;
- a configuration register ~~means~~ storing configuration data for the FIFO buffer;
- a read control ~~means~~ for controlling the read-out of the FIFO buffer; and
- a bus command unit ~~means~~ for receiving control of the system bus and providing an address for the data read-out from the FIFO buffer ~~means~~.

8. (Currently amended) An interface as claimed in claim 1 wherein the memory ~~means~~ is an addressable memory.

9. (Currently amended) An interface as claimed in claim 8 wherein the signal generator ~~means~~ generates an interrupt signal for transmission to the processor system.

10. (Currently amended) An interface as claimed in claim 9 wherein the circuit ~~means~~ for controlling the transfer of the data includes:

- a command decoder ~~means~~ for receiving address and command signals from the processor system;
- a configuration register ~~means~~ for storing configuration data for the addressable memory; and
- a read control ~~means~~ for controlling the read-out of the addressable memory.

11. (Currently amended) An interface as claimed in claim 10 wherein the interface further includes an array register ~~means~~ for determining the dimension of the imaging array data.

12. (Currently amended) An interface as claimed in claim 8 wherein the signal generator ~~means~~ generates a bus request signal for transmission to a bus arbitration unit for the processor system.

13. (Currently amended) An interface as claimed in claim 12 wherein the circuit ~~means~~ for controlling the transfer of the data further includes:

- a command decoder ~~means~~ for receiving address and command signals from the processor system;
- a configuration register ~~means~~ storing configuration data for the addressable memory;
- a read control ~~means~~ for controlling the read-out of the addressable memory; and
- a bus command unit ~~means~~ for receiving control of the system bus and providing an address for the data read-out from the addressable memory.

14. (Currently amended) An interface as claimed in claim 13 wherein the interface further includes an array register ~~means~~ for determining the dimension of the imaging array data.

15. (Currently amended) An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus comprising:

- an imaging array sensor having an array of sensing pixels and an array address generator integrated on a die; and
- an interface ~~means~~ integrated on the die for receiving data from the imaging array sensor as determined by the imaging array sensor and adapted to transfer the data to the electronic processing system as determined by the electronic processing system.

16. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim 15 where the interface ~~means~~ includes:

- a memory ~~means~~ for storing imaging array data and address signals at a rate determined by the imaging array sensor; and
- a circuit ~~means~~ for controlling the transfer of the data from the memory ~~means~~ to the data bus at a rate determined by the electronic processing system.

17. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory ~~means~~ includes a first-in first-out (FIFO) buffer.

18. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration ~~means~~ unit coupled to the circuit ~~means~~ for controlling the transfer of the data.

19. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim 17 which further includes a bus arbitration ~~means~~ unit integrated on the die and coupled to the circuit ~~means~~ for controlling the transfer of the data.

20. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory ~~means~~ includes an addressable memory.

21. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim 20 which further includes a bus arbitration ~~means~~ unit coupled to the circuit ~~means~~ for controlling the transfer of the data.

22. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim 20 which further includes a bus arbitration ~~means~~ unit integrated on the die and coupled to the circuit ~~means~~ for controlling the transfer of the data.

23. (Currently amended) An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus comprising:

- an imaging array of sensing pixels;
- a buffer ~~means~~ for storing data received at an input port and for outputting data through an output port to the data bus;
- ~~means~~ a unit for transferring data from a selected pixel to the buffer input port;
- a counter ~~means~~ for determining the quantity of data in the buffer ~~means~~;
- a signal generator ~~means~~ for alerting the electronic processing system when the quantity of data in the buffer ~~means~~ attains a predetermined level; and
- ~~means~~ a circuit adapted to respond to the electronic processing system for controlling the transfer of the stored data through the buffer ~~means~~ output port.

24. (Currently amended) An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus and a system address/control bus comprising:

- an imaging array of sensing pixels;
- a buffer ~~means~~ for storing data received at an input port and for outputting data through an output port to the data bus;
- ~~means~~ a unit for transferring data from a selected pixel to the buffer input port;
- ~~means~~ a counter for determining the quantity of data in the buffer ~~means~~;
- ~~means~~ a signal generator for seeking control of the data bus when the quantity of data in the buffer ~~means~~ attains a predetermined level; and
- ~~means~~ a circuit adapted to respond to the availability of the data bus for controlling the transfer of the stored data through the buffer ~~means~~ output port.

25. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim 24 which includes a bus arbitration unit ~~means~~ for receiving data bus control requests and for providing data bus control in response to a request.

26. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim 25 wherein the ~~means~~ circuit for responding to the availability of the data bus includes:
- ~~means~~ an address unit for storing and incrementing destination addresses; and
- ~~means~~ a bus command unit for asserting the destination address and write controls on the system address/control bus.

27. (Currently amended) An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus comprising:
- an imaging array of sensing pixels;

- memory ~~means~~ having a plurality of memory cells arranged in rows and columns for storing data received at an input port and for outputting data through an output port to the data bus;
- ~~means~~ a unit for transferring data from a selected pixel to a selected memory cell through the memory ~~means~~ input port;
- ~~means~~ a counter for determining the quantity of data in the memory ~~means~~;
- ~~means~~ a signal generator for alerting the electronic processing system when the quantity of data in the memory ~~means~~ attains a predetermined level; and
- ~~means~~ a circuit adapted to respond to the electronic processing system for controlling the transfer of the stored data through the memory ~~means~~ output port.

28. (Currently amended) An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus and a system address/control bus comprising:
- an imaging array of sensing pixels;
- memory ~~means~~ having a plurality of memory cells arranged in rows and columns for storing data received at an input port and for outputting data through an output port to the data bus;
- ~~means~~ a unit for transferring data from a selected pixel to a selected memory cell through the memory input port;
- ~~means~~ a counter for determining the quantity of data in the memory ~~means~~;
- ~~means~~ a signal generator for seeking control of the data bus when the quantity of data in the memory ~~means~~ attains a predetermined level; and
- ~~means~~ a circuit adapted to respond to the availability of the data bus for controlling the transfer of the stored data through the memory ~~means~~ output port.

29. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim ~~24~~ 28 which includes a bus arbitration unit ~~means~~ for receiving data bus control requests and for providing data bus control in response to a request.

30. (Currently amended) An integrated semiconductor imaging circuit as claimed in claim ~~25~~ 29 wherein the ~~means~~ circuit for responding to the availability of the data bus includes:

- ~~means~~ an address unit for storing and incrementing destination addresses; and
- ~~means~~ a bus command unit for asserting the destination address and write controls on the system address/control bus.